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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,942	03/16/2004	Charles H. Moore	0057-011	2932

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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,942	MOORE, CHARLES H.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 are pending.

Papers Filed

2. Examiner acknowledges receipt of amendments and remarks filed on 11 November 2006.

Title

3. The title is accepted. Objection is withdrawn.

Drawings

4. Objections are withdrawn.

Claim Objections

5. Claims are objected to because of the following informalities:

Claim 1: the added "and" appears to be redundant. The claim, as currently amended, reads "a plurality of computers; and and a plurality of data paths"

6. Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. Rejection is withdrawn.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 40-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the terms "substantially the same" and "mirror image" are indefinite.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4, 6-7, 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hogenauer (US Publication No. 2003/0028750).

10. As per claim 1, Hogenauer teaches a computer array, comprising: a plurality of computers (Fig. 1 matrices 150); and a plurality of data paths connecting the computers (Fig. 1 interconnection network 110); the data paths being hard wired between

associated pairs of computers; wherein: at least some of the computers are assigned a task different from that assigned to the other computers. (Paragraph 4)

"Hardwired" is defined as "computer or computer controlled system which functions by means of fixed or committed circuitry." This does not appear to require the dedicated connection that Applicant has amended into other claims.

11. As per claim 2, Hogenauer teaches the computer array of claim 1, wherein: each of the computers is assigned a task different from that of the other computers. (Paragraph 4)

12. As per claim 3, Hogenauer teaches the computer array of claim 1, wherein: at least some of the computers are configured for specific input functions. *The examiner asserts that each and every matrix must inhernetly be able to input data. Without input data, the processor could not perform any function.*

13. As per claim 4, Hogenauer teaches the computer array of claim 1, wherein: at least some of the computers are configured for specific output functions. *The examiner asserts that Hogenauer's processor must inherently contain at least one matrix which can output data, as indicated in Fig. 1. Further, a processor which cannot output data can perform no useful function.*

14. As per claim 6, Hogenauer teaches the computer array of claim 1, wherein: communication between the computers is via a plurality of parallel data lines. *Paragraph 5 discloses the system to be a multi-bit system, which defines the data bus to be of a size greater than one bit.*

15. As per claim 7, Hogenauer teaches the computer array of claim 1, wherein: each of the computers is hard wired to communicate with at least three of the plurality of computers. *The examiner asserts that, as shown in Fig. 1, each matrix may communicate with each other matrix by means of the interconnection network 110.*

16. As per claim 12, Hogenauer teaches the computer array of claim 1, wherein: at least one of the computers is in direct communication with an external memory source. *As shown in Fig. 1, each matrix is connected directly to memory 140 by means of interconnection network 110.*

17. As per claim 13, Hogenauer teaches the computer array of claim 1, wherein: at least one of the computers communicates data from an external memory source to at least some of the plurality of computers. *The examiner asserts that, as shown in Fig. 1, memory 140 is external to the matrix processing blocks.*

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4, 6-7, 12-14, 17-21, and 23-28, 34, 40-41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogenauer in view of Baxter (U.S. Patent No. 6,460,128).

2. Claims 1-4, 6-7, and 12-13 are rejected for the same reasons as shown above. The additional reference of Baxter was used to anticipate what Examiner believes was Applicant's intended meaning of the term "hard wired".

Hogenauer fails to disclose dedicated wiring exclusively between two computers of the array.

Baxter discloses transfer of information between nodes through a dedicated bus (col 3 lines 34-38).

As described in col 3 lines 34-38, Hogenauer would have been motivated to utilize this technique to avoid bus contention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hogenauer and allow processing nodes to communicate through dedicated lines as suppored by Baxter.

19. Claim 14 is directed to a method implementing the details of the array of claim 1 and is rejected under the same grounds.

20. Claim 17 is directed to a method implementing the details of the array of claims 3 and 4 and is rejected under the same grounds.

21. As per claim 18, Hogenauer/Baxter teaches the method of claim 14, wherein: one of the computers routes assignments to the remainder of the computers. (Hogenauer Paragraph 15)

22. Claim 19 is directed to an array implementing the details of the array of claim 1 and is rejected under the same grounds.

23. As per claim 20, Hogenauer/Baxter teaches the computer array of claim 19, wherein: the different functions work together to accomplish a task. *Hogenauer's processor inherently accomplishes a task, depending on what it is programmed to do. The processors execute different portions of the task (Hogenauer paragraph 4).*

24. As per claim 21, Hogenauer/Baxter teaches the computer array of claim 19, wherein: each of the functions is programmed into the respective computers when the computer array is initialized. *The examiner asserts that the matrices must inherently be*

programmed once processing is initialized. If it weren't, the processor would be unable to accomplish its assigned task.

25. Claim 23 is directed to a method implementing the details of the array of claims 1 and 21 and is rejected under the same grounds.

26. As per claim 24, Hogenauer/Baxter teaches the method for accomplishing a task of claim 23, wherein: the operational components are operations used in accomplishing a global positioning system receiver. (Baxter Paragraph 2)

27. Claim 25 is directed to a method implementing the details of the array of claim 21 and is rejected under the same grounds.

28. As per claim 26, Hogenauer/Baxter teaches the method for accomplishing a task of claim 23, wherein: the computers are arranged in a computer array. (Hogenauer Fig. 1)

3. As per claim 27, Hogenauer/Baxter teaches the method of claim 1, wherein: at least some of the data paths are connected to no more than two of the computers (Baxter col 3 lines 34-38).

4. As per claim 28, Hogenauer/Baxter teaches the method of claim 1, wherein: each of the data paths is dedicated to an adjacent pair of computers (Baxter col 3 lines 34-38).

Note that the American Heritage Dictionary defines adjacent as "close to; lying near".

5. As per claim 34, Hogenauer/Baxter teaches the method of claim 1, wherein: each of the computers is an independently functioning computer (Hogenauer paragraph 4).

6. As per claims 40-41, Hogenauer/Baxter teaches the method of claim 1, wherein the computers are "substantially the same" and "mirror images of adjacent computers".

7. As per claim 43, Hogenauer/Baxter discloses a computer array, comprising: a plurality of computers (fig. 1 reference 150), and a plurality of data paths connecting the computers (fig. 1 reference 110); and wherein at least some of the computers are assigned a task different from the assigned to the other computers (paragraph 4)

29. Claims 5, 8-11, 15-16, 22, 29, 35 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogenauer/Baxter in view of common art.

30. As per claim 5, Hogenauer/Baxter teaches the computer array of claim 1, but fails to disclose wherein: communication between the computers is asynchronous.

31. Official Notice is taken that asynchronous communication is well known in the art. Asynchronous communication provides the benefit of not having to provide a single clock signal to multiple elements, eliminating wiring and decreasing physical size of the logic.

32. It would have been obvious to one of ordinary skill in the art at the time of invention to have included asynchronous communication lines between Hogenauer's matrices 150 for the benefit of decreased wiring and physical logic size.

8. As per claim 29, Hogenauer/Baxter teaches the method of claim 1, wherein: the computers operate asynchronously.

9. As per claim 35, Hogenauer/Baxter teaches the method of claim 1, wherein: the computers operate asynchronously; and the computers communicate with each other asynchronously.

Note: since the computers communicate asynchronously, the are considered to operate asynchronously for that reason.

10. As per claim 44, Hogenauer/Baxter teaches the method of claim 43, wherein: the computers communicate with each other asynchronously.

33. As per claim 8, Hogenauer/Baxter teaches the computer array of claim 1, but fails to disclose wherein: the quantity of computers is 25.

34. Official Notice is taken that modifying the number of processors in the system is well known in the art. Increasing the number of processors would increase the throughput of execution.

35. It would have been obvious to one of ordinary skill in the art at the time of invention to have included 25 matrices in Hogenauer's processor for the benefit of increased processing throughput.

36. As per claim 9, Hogenauer/Baxter teaches the computer array of claim 1, but fails to disclose wherein: the computers are physically arrayed in a 5 by 5 array.

37. Official Notice is taken that modifying the number and arrangement of processors is well known in the art. A five by five array provides more processors, therefore increased processing throughput.

38. It would have been obvious to one of ordinary skill in the art at the time of invention to have increased the number of matrices in Hogenauer's processor and to have arranged them in a five by five array for the benefit of increased processing throughput.

39. Further, as shown in In re Japikse, 86 USPQ 70 (CCPA 1950), shifting location of parts is generally not given patentable weight or would have been obvious improvements.

40. As per claim 10, Hogenauer/Baxter teaches the computer array of claim 1, but fails to teach wherein: at least some of the computers are physically arrayed in a 4 by 6 array.

41. Official Notice is taken that modifying the number and arrangement of processors is well known in the art. A four by six array provides more processors, therefore increased processing throughput.

42. It would have been obvious to one of ordinary skill in the art at the time of invention to have increased the number of matrices in Hogenauer's processor and to have arranged them in a four by six array for the benefit of increased processing throughput.

43. Further, as shown in In re Japikse, 86 USPQ 70 (CCPA 1950), shifting location of parts is generally not given patentable weight or would have been obvious improvements.

44. As per claim 11, Hogenauer/Baxter teaches the computer array of claim 1, but fails to teach wherein: the quantity of computers along each side of the array is an even number.

45. Official Notice is taken that arranging processors in an array with multiple rows and columns is well known in the art. An array with multiple rows and columns decreases interconnection length between processors.

46. It would have been obvious to one of ordinary skill in the art at the time of invention to have arranged Hogenauer's four matrices in a grid formation of two by two to decrease interconnection length between the matrices.

47. Further, as shown in In re Japikse, 86 USPQ 70 (CCPA 1950), shifting location of parts is generally not given patentable weight or would have been obvious improvements.

48. As per claim 15, Hogneauer/Baxter teaches the method of claim 14, wherein: at least one of the computers is assigned to communicate with a memory, but fails to teach flash memory.

49. Official Notice is taken that flash memory is well known in the art. Flash memory provides quick storage and retains values after power has been removed from the memory.

50. It would have been obvious to one of ordinary skill in the art at the time of invention to have used flash memory for memory 140 in Hogenauer's processor for the benefit of retaining information after power had been shut off.

51. As per claim 16, Hogenauer/Baxter teaches the method of claim 14, wherein: at least one of the computers is assigned to communicate with a memory, but fails to teach random access memory.

52. Official Notice is taken that random access memory (RAM) is well known in the art. RAM provides a method of storing large amounts of data at a low cost.

53. It would have been obvious to one of ordinary skill in the art at the time of invention to have used RAM as memory 140 in Hogenauer's processor.

54. Claim 22 is directed to an array implementing the details of the array of claim 5 and is rejected under the same grounds.

Claims 30-33, 36-38, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogenauer/Baxter in view of Dokie (U.S. Patent No. 6,101,598).

Regarding claims, 30-33, 36-38 and 42, Hogenauer/Baxter discloses the method of claim 1 and the elements of claim 42 shown with regard to claim 43.

Hogenauer/Baxter fails to disclose dedicated RAM and ROM for particular processors.

Dokie discloses dedicated RAM and ROM for processors in a multiple processor system (fig. 2).

Hogenauer/Baxter would have been motivated to utilize the dedicated RAM/ROM of Dokie to avoid contention between memory addresses and memory buses.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hogenauer/Baxter and incorporate the local RAM and ROM of Dokie.

11. As per claim 30-33, Hogenauer/Baxter teaches the method of claim 1, wherein: each of the computers includes dedicated memory of RAM and ROM.

12. As per claim 36-38, Hogenauer/Baxter teaches the method of claim 1, wherein: each of the computers includes dedicated memory of RAM and ROM

13. As per claim 42, Hogenauer/Baxter discloses a computer array, comprising: a plurality of computers (fig. 1 reference 150), and a plurality of data paths connecting the computers (fig. 1 reference 110); and wherein at least some of the computers are assigned a task different from the assigned to the other computers (paragraph 4) and at least some of the computers included dedicated memory for the exclusive use of an associated one of the computers.

14. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hogenauer/Baxter in view of Glass (U.S. Patent No. 5,784,602).

As per claim 39, Hogenauer/Baxter discloses the computer array of claim 1 but fails to disclose that the computers are integrated in a single unitary substrate. Glass discloses a system on an integrated circuit (col 4 lines 21-25).

At the time of the invention, one skilled in the art would have been motivation to make the combination based on the reasoning disclosed in Glass that an integrated circuit "is highly advantageous for space, speed, power consumption and cost reasons" (col 4 lines 23-25)

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computer array of Hogenauer/Baxter and combine it to a single integrated circuit as disclosed in Glass.

Response to Arguments

15. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. Other arguments are addressed below.

16. Applicant desires a reference supporting the Official Notice of asynchronous communications within an array processor. Nakagoshi (U.S. Patent No. 5,377,333) has been provided. Applicant's attention is directed to col 19 lines 24-37.

17. Applicant desires references supporting the Official Notice of 5X5 and 4X6 configurations of an array and believes In re Japiske to not be relevant in this case. Ikenaga (U.S. Patent No. 6,154,809) Fig 31 and Morris (U.S. Patent No. 6,085,304) col 4 line 7 have been provided for 5X5 and 4X6 arrays respectively.

Additionally, Applicant's disclosure of 4X6 and 5X5 arrays appears to represent a mere example of possible configurations. In fact, page 7 Lines 7-11 discloses "It should be noted that, as with the view of Fig. 1, the view of Fig. 3 is not intended as a layout diagram and, therefore, is not intended to indicate a necessary physical placement of any of the computers 12. Nevertheless, the example of Fig. 3 is indicative of the fact that it is thought that the 5 by 5 computer array 10a is a useful physical arrangement of

the computers 12". This statement supports that the use of 4X6 and 5X5 arrays is an obvious change based on specific implementation and is not essential for the invention. *See In re Kuhle*, 526 F.2d 553, 555, 188 USPQ 7,9 (CCPA 1975).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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